

Fig. 1

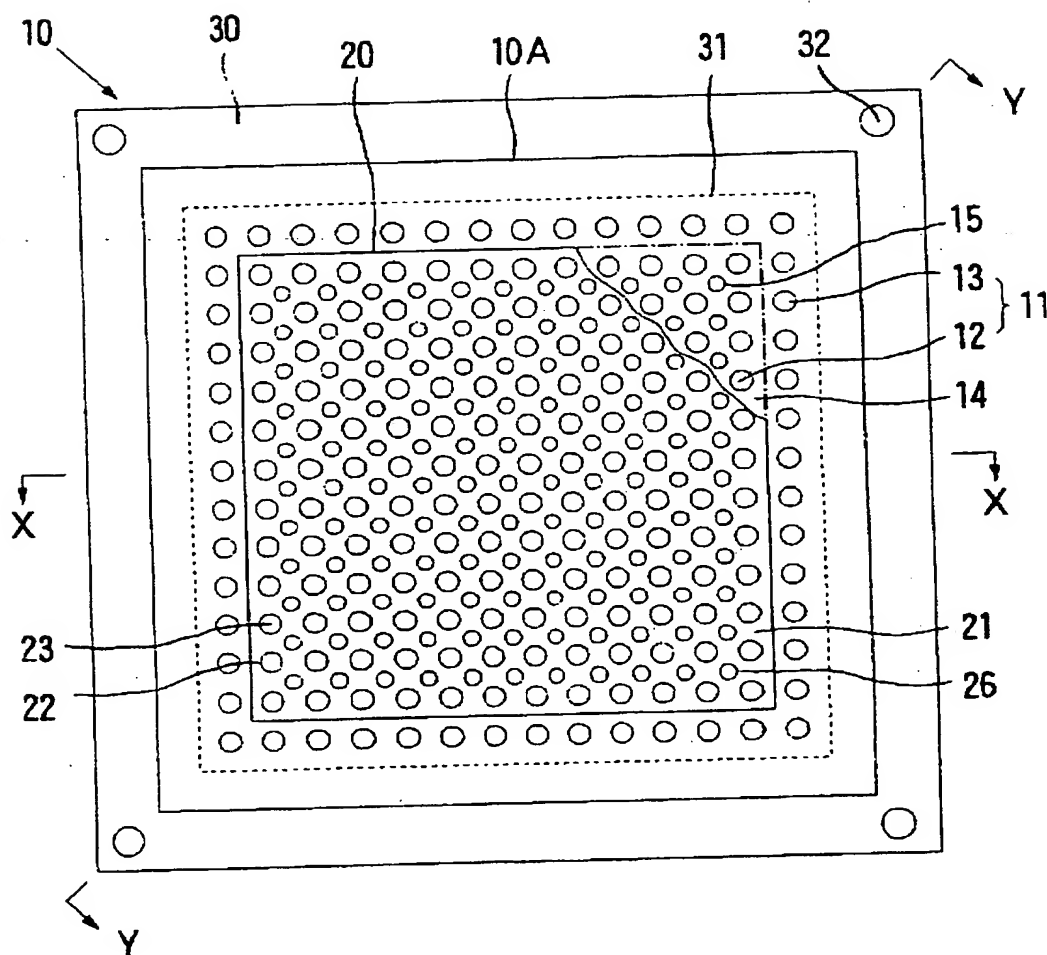


Fig. 2

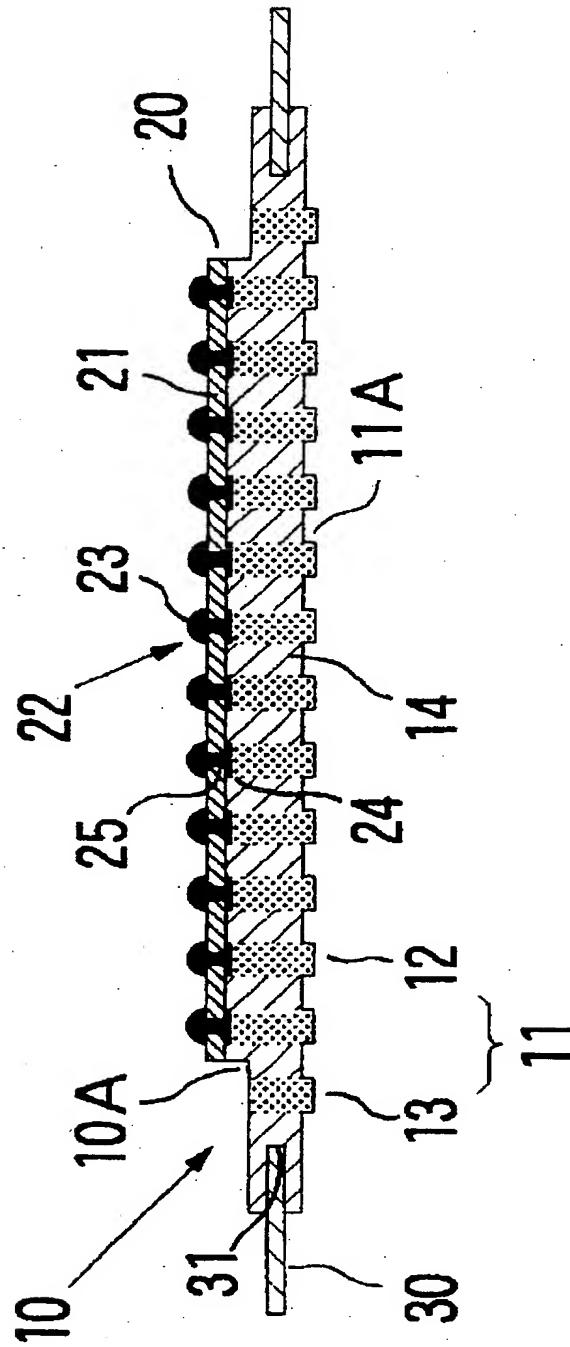


Fig. 3

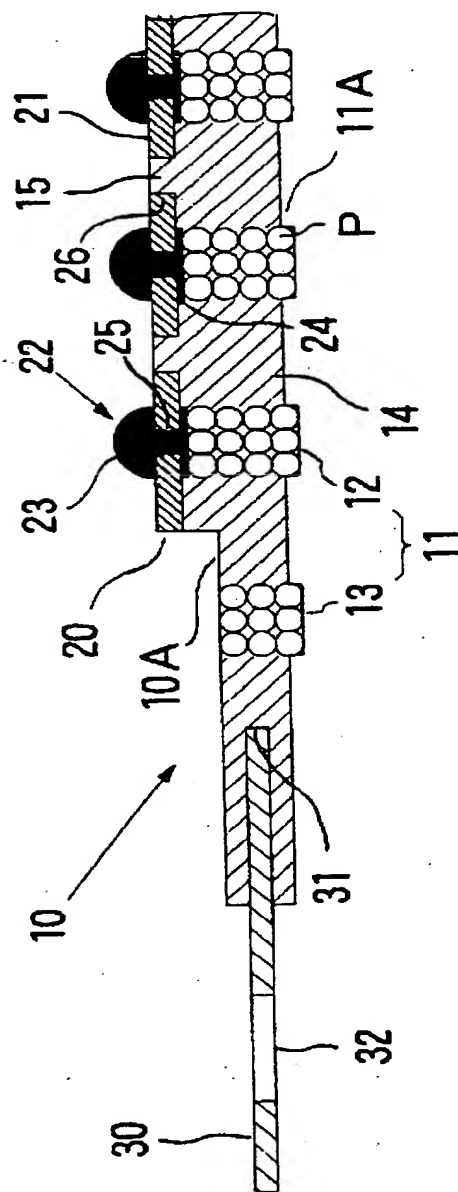


Fig. 4

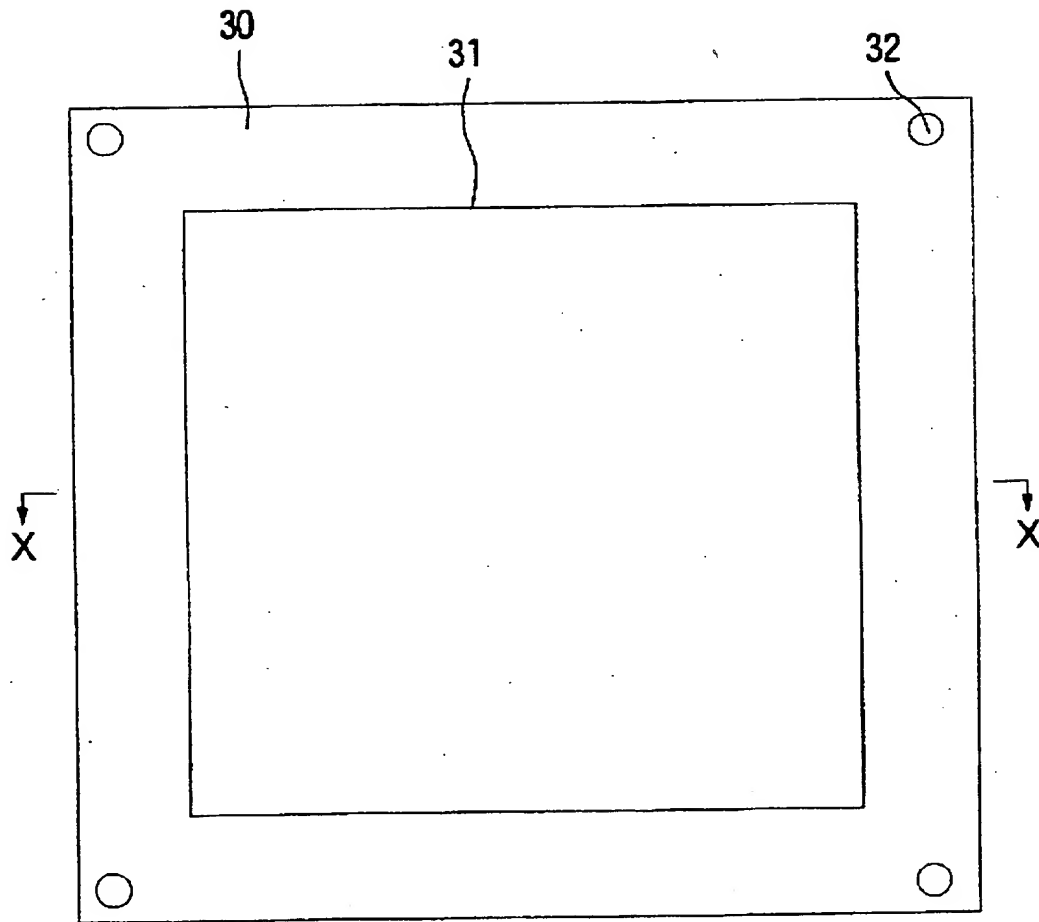


Fig. 5

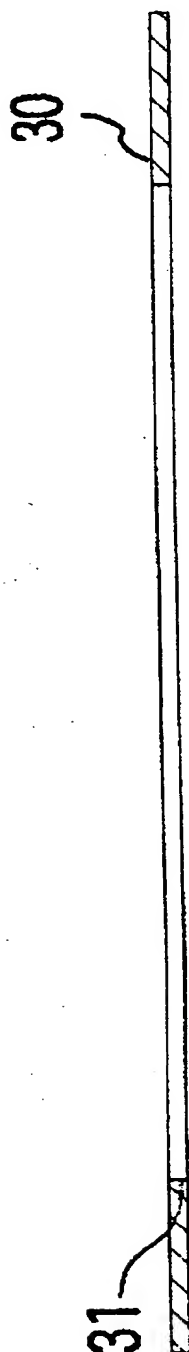


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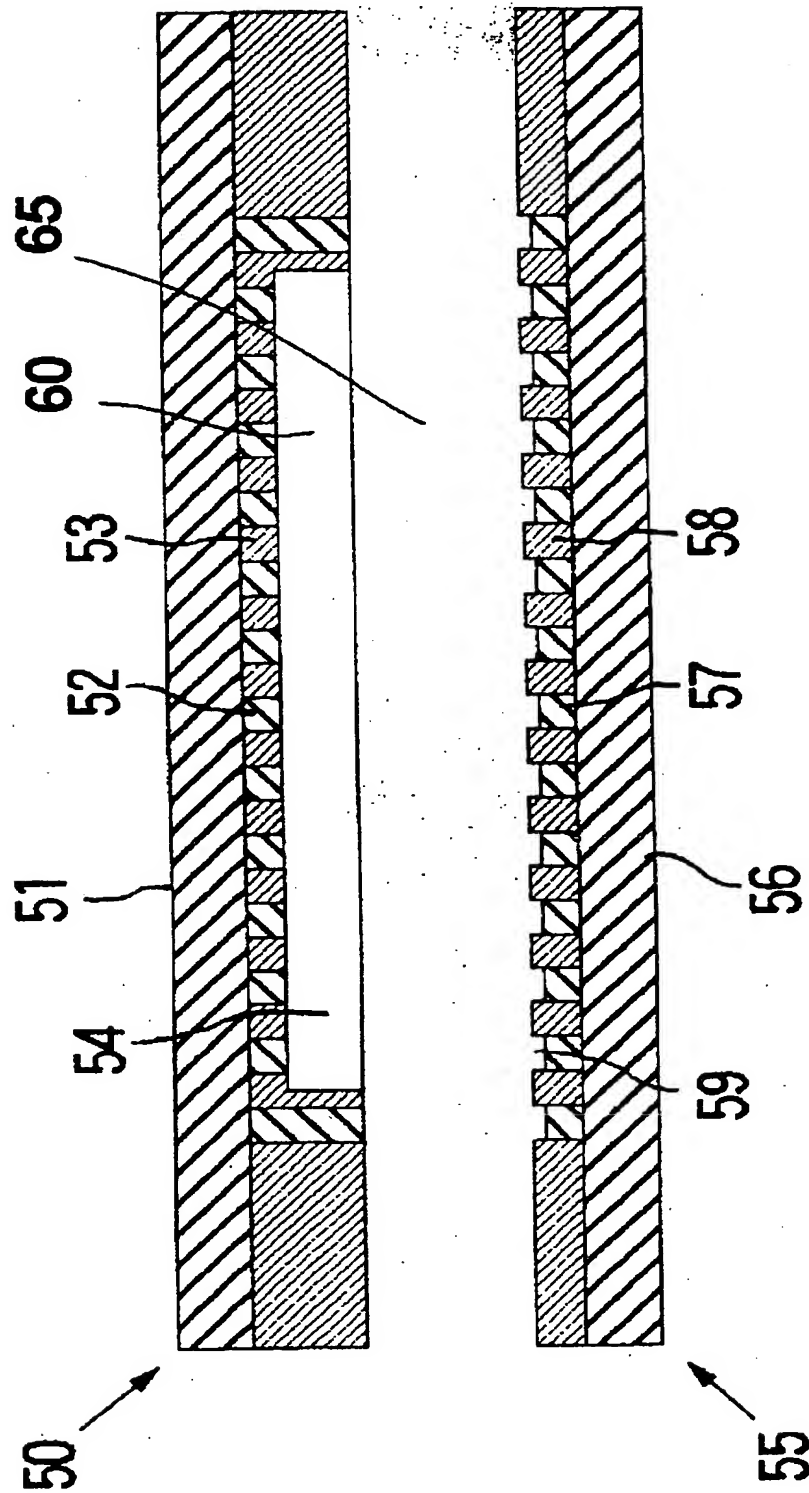


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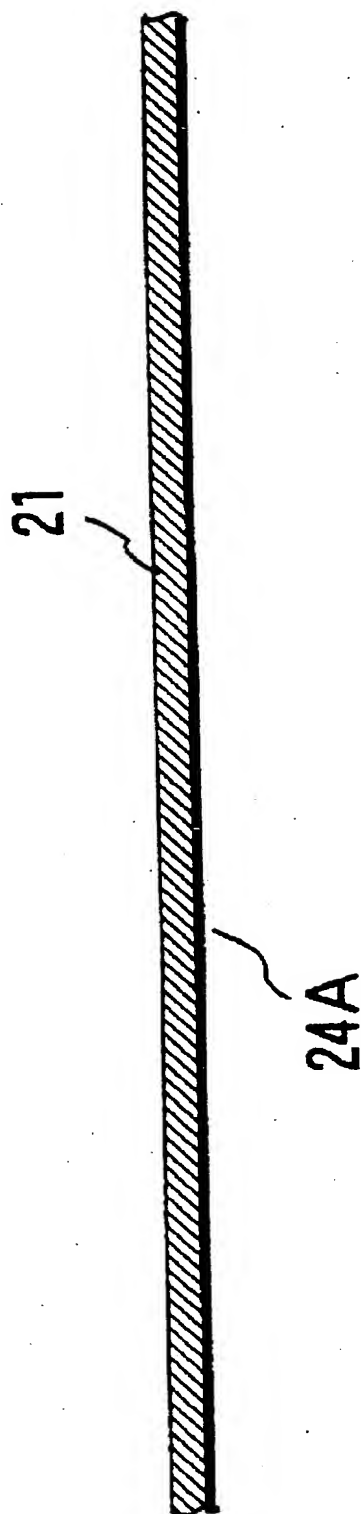


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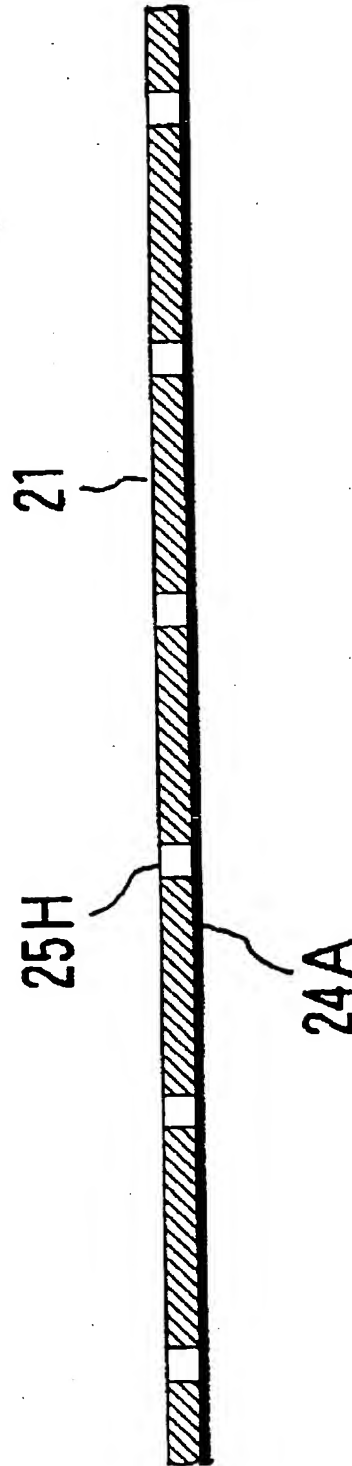


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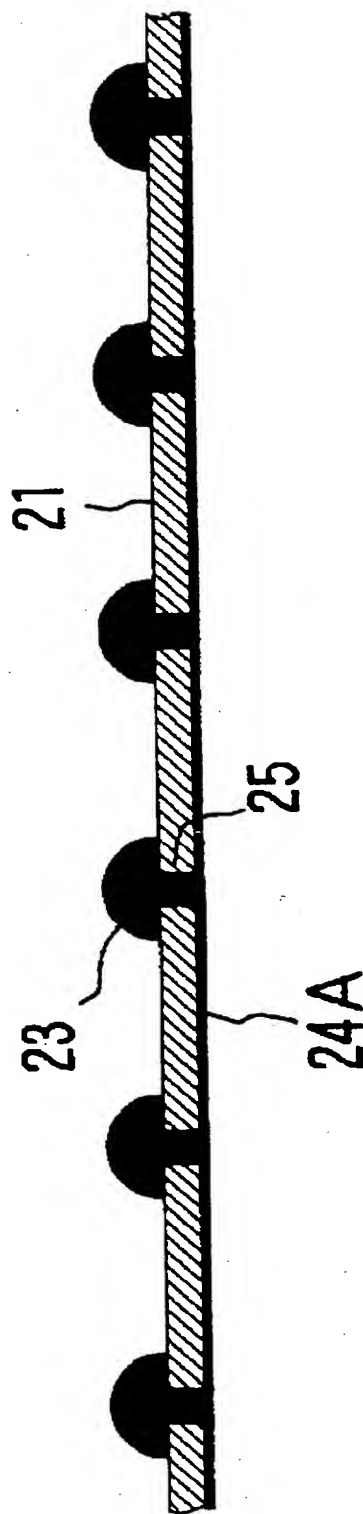


Fig. 10

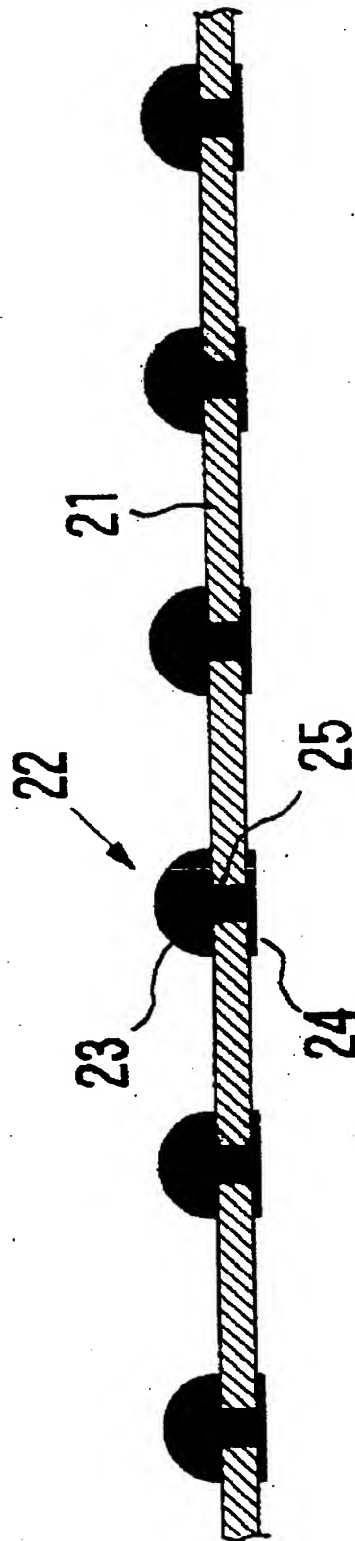


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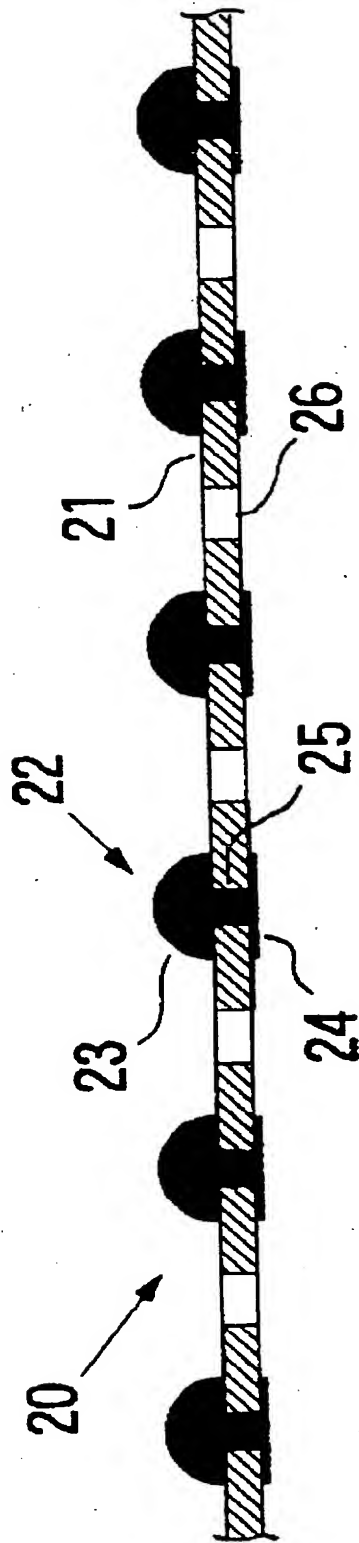


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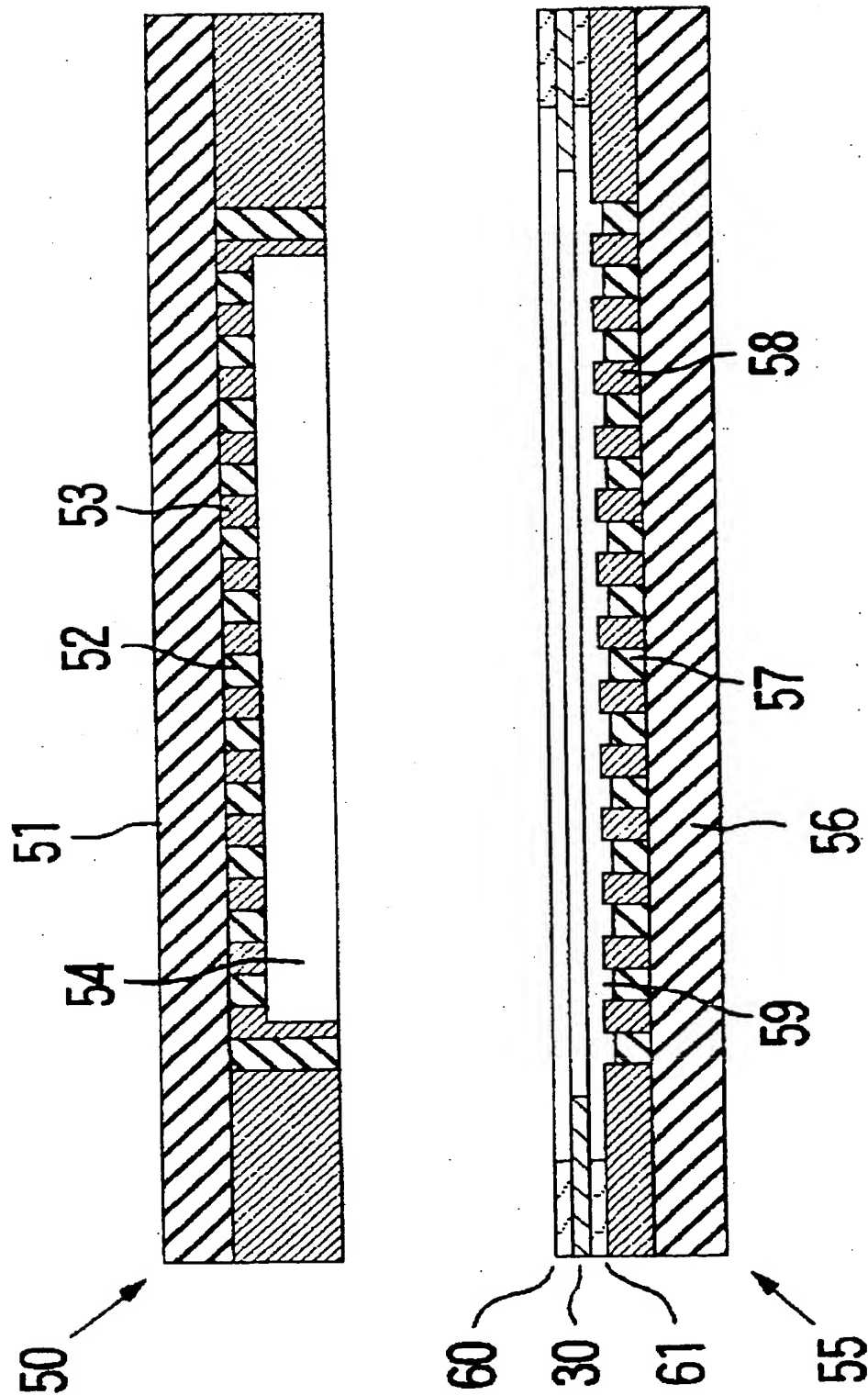


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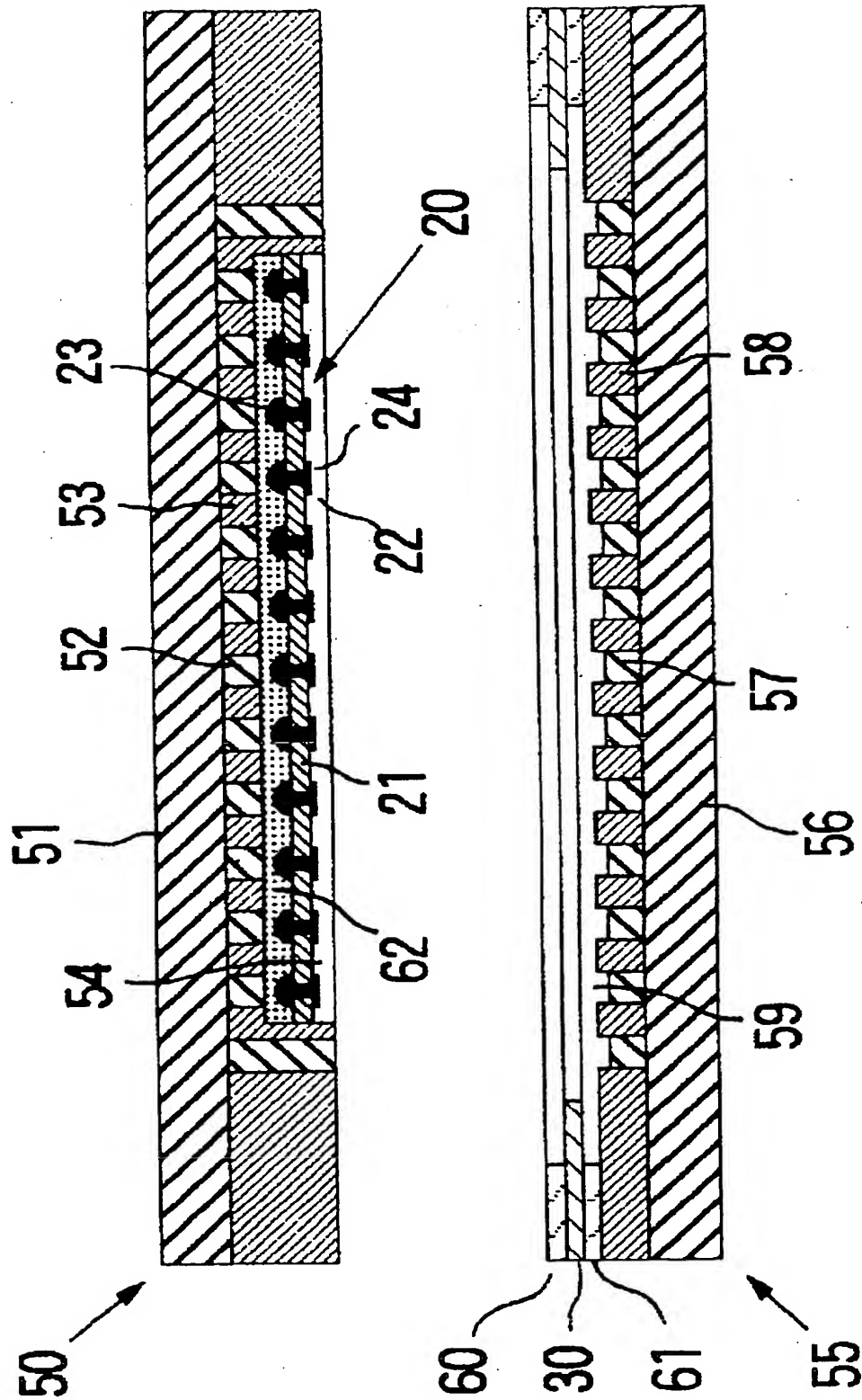


Fig. 14

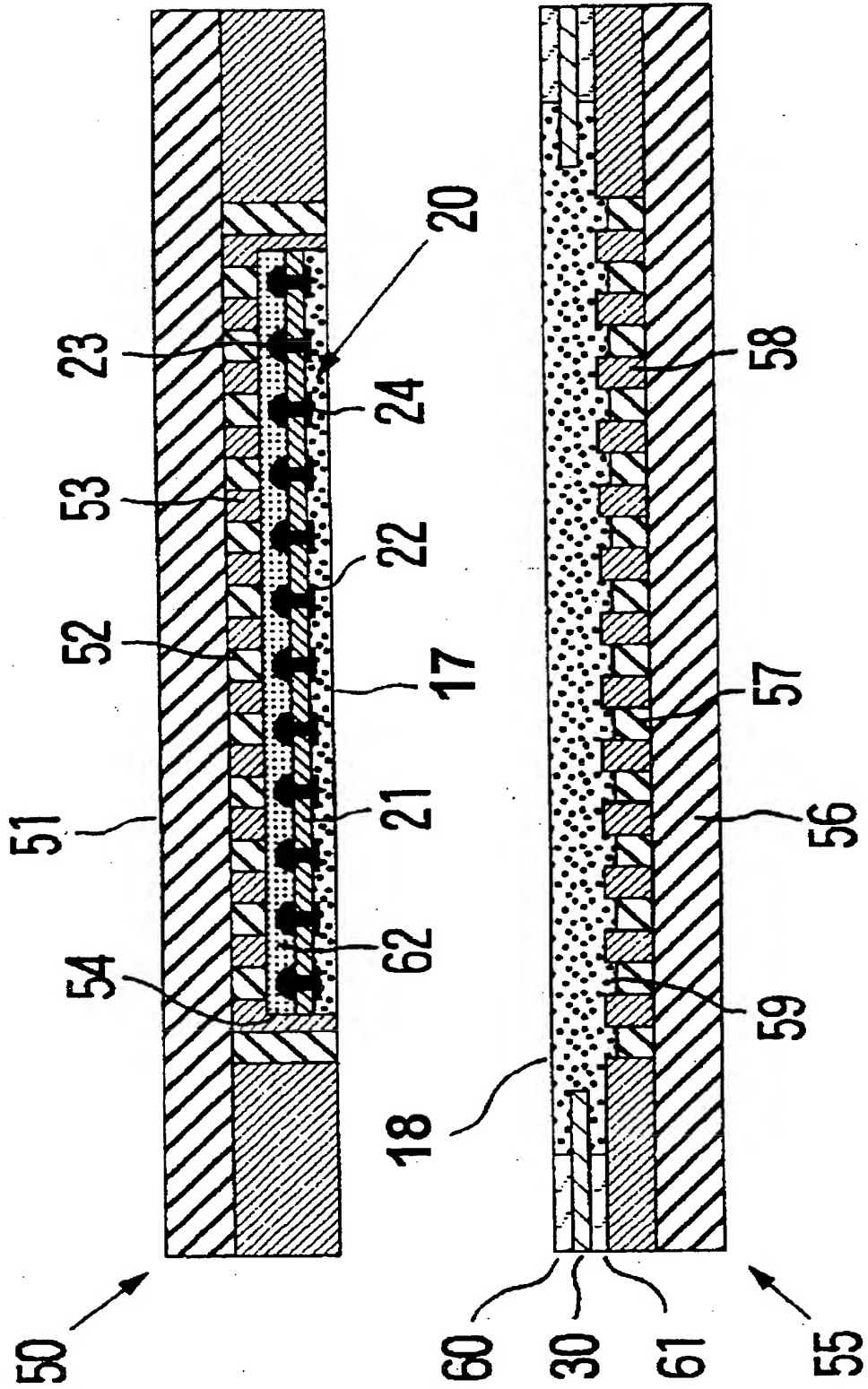


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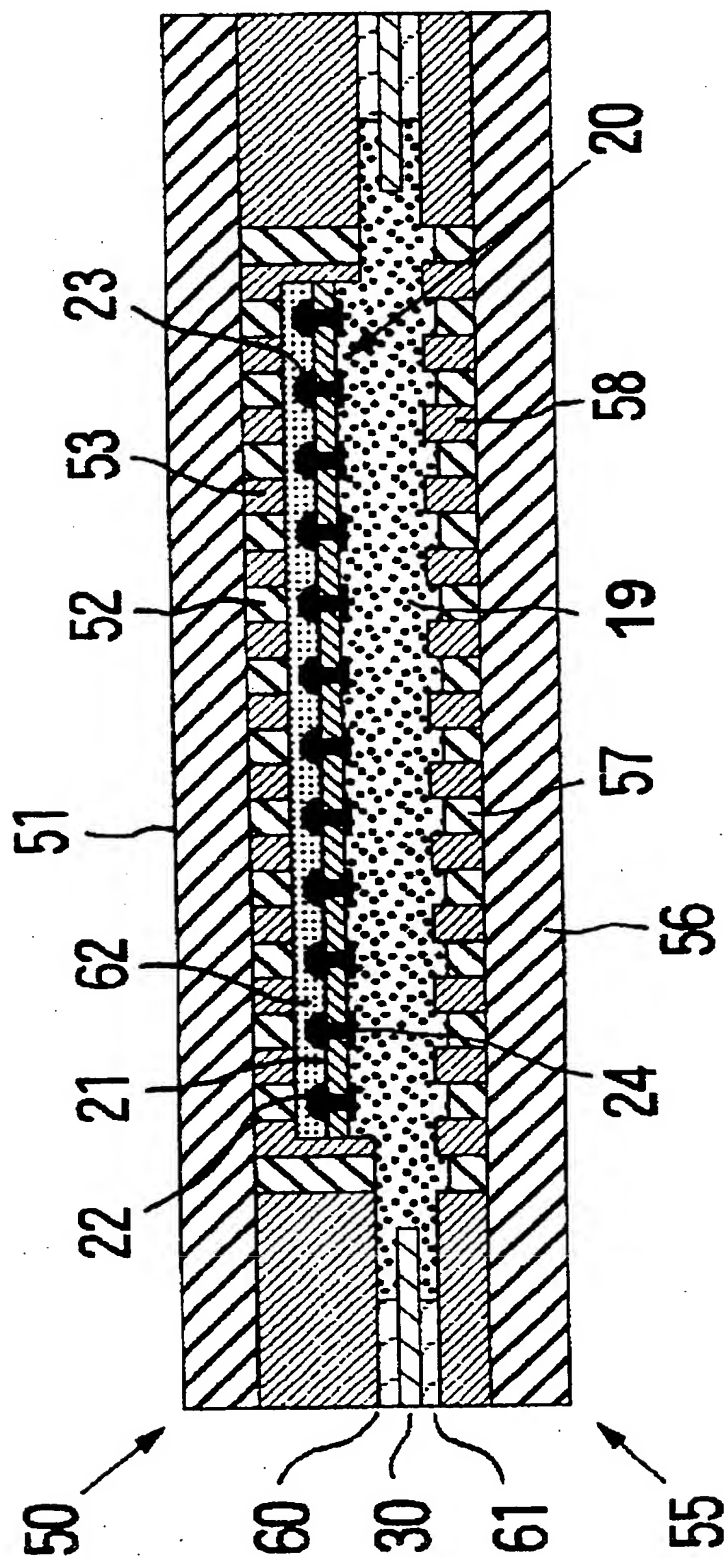


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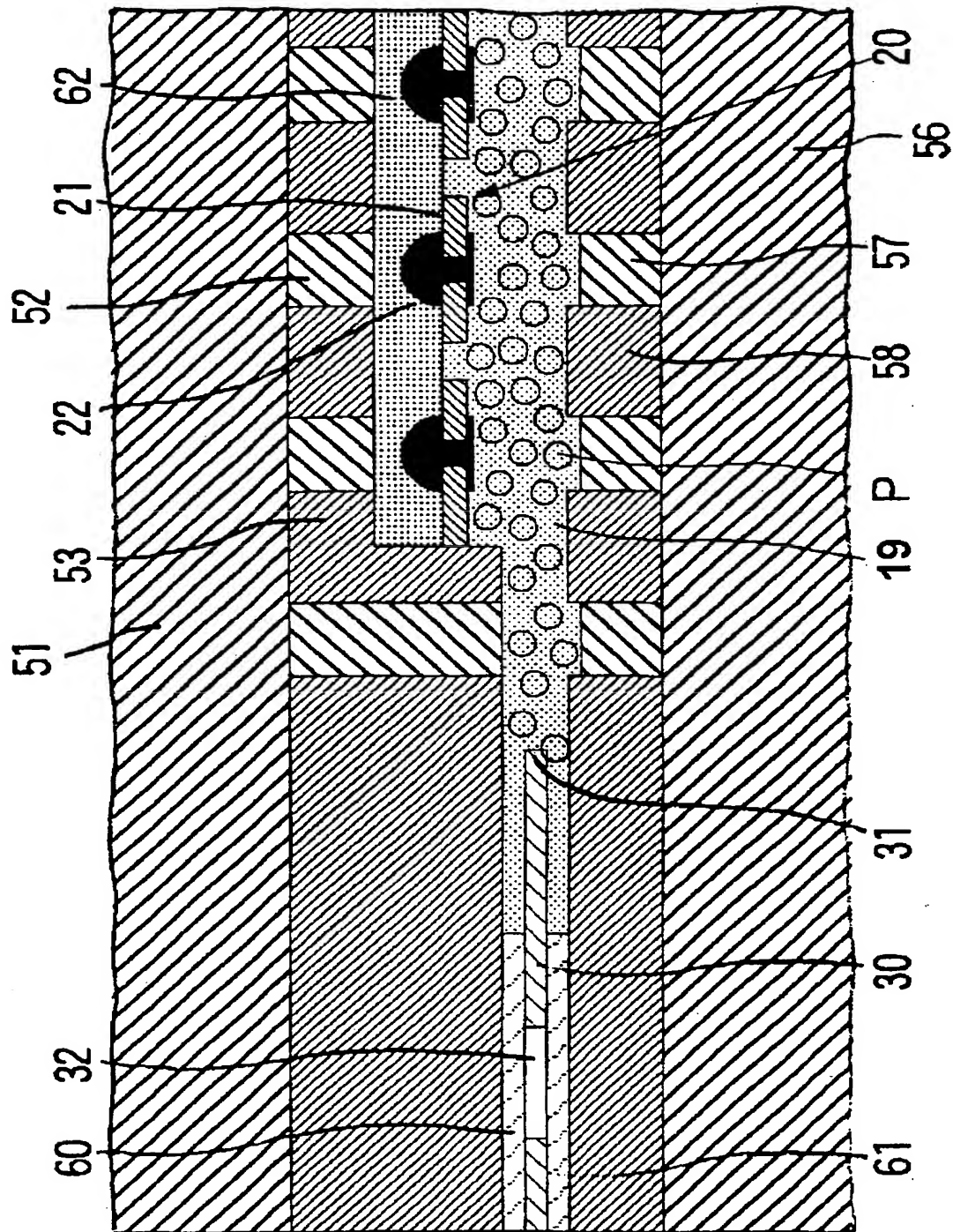


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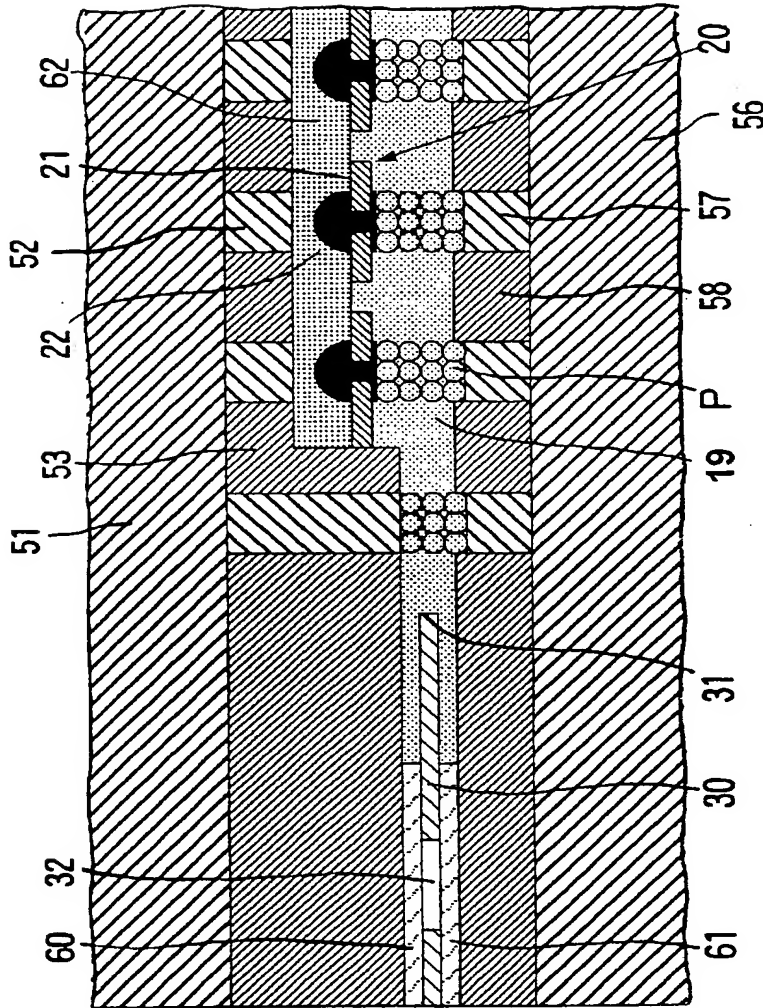


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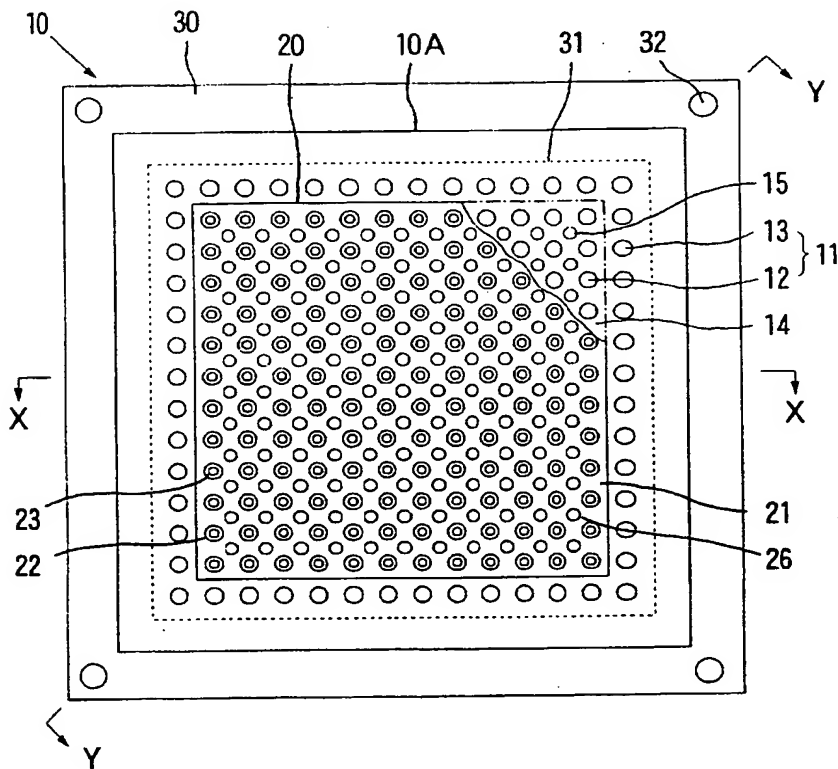


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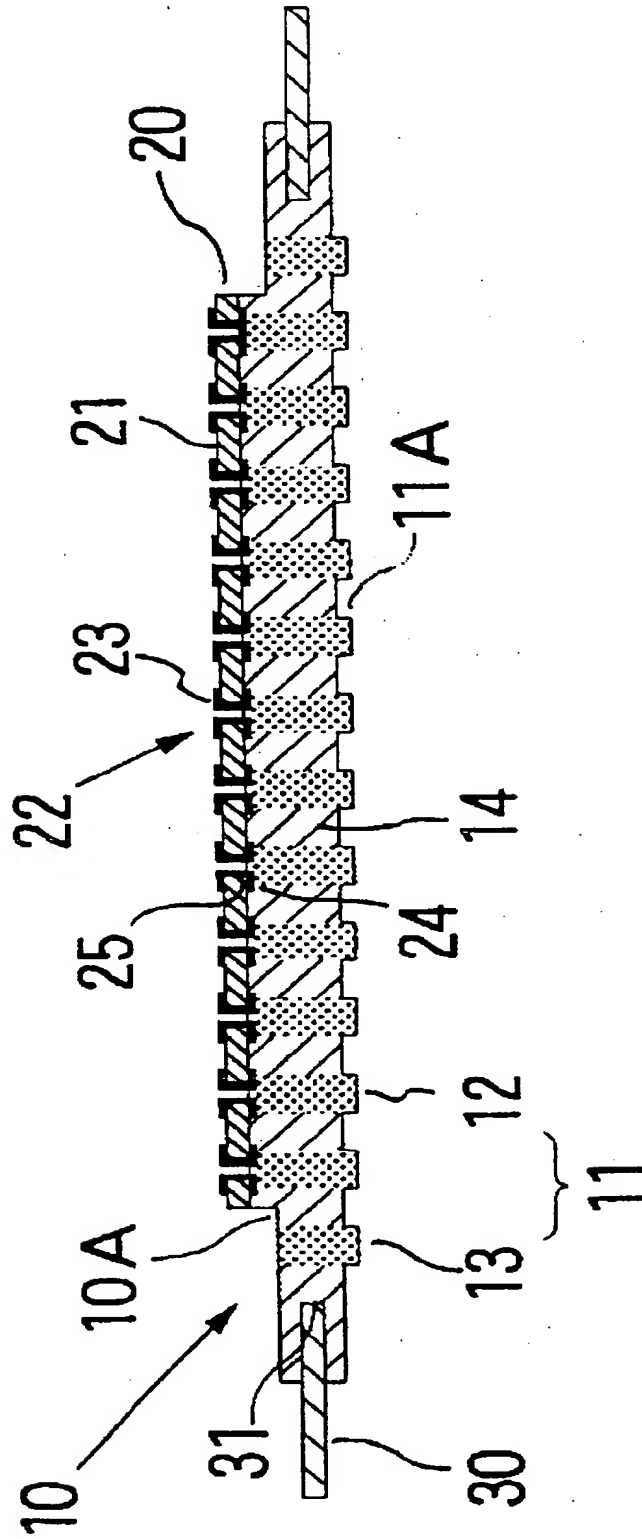


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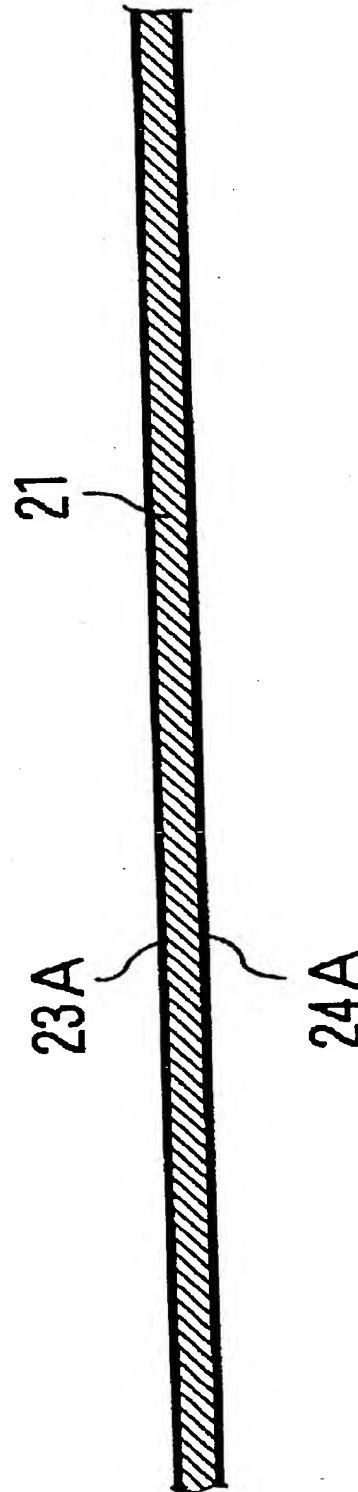


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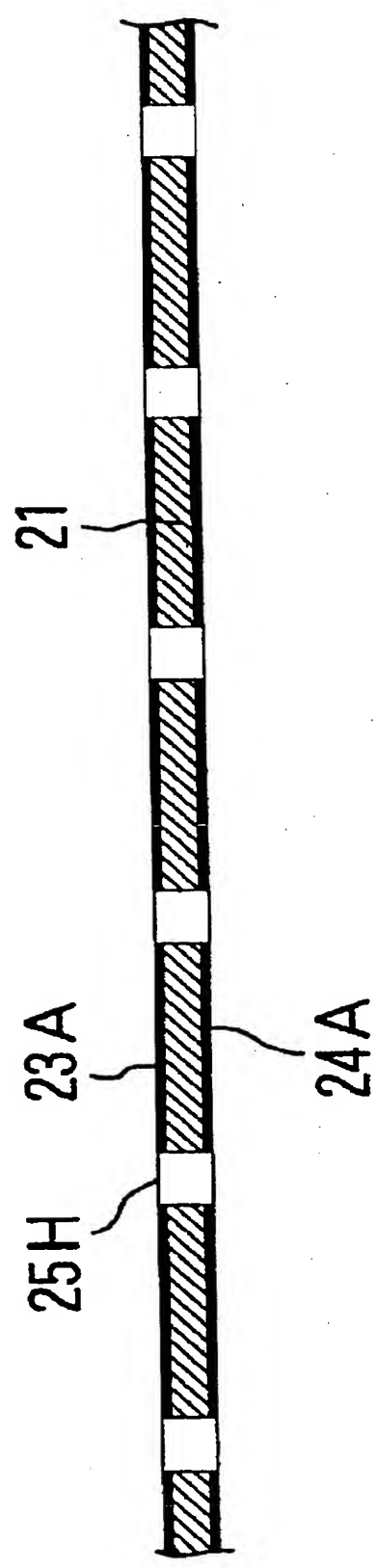


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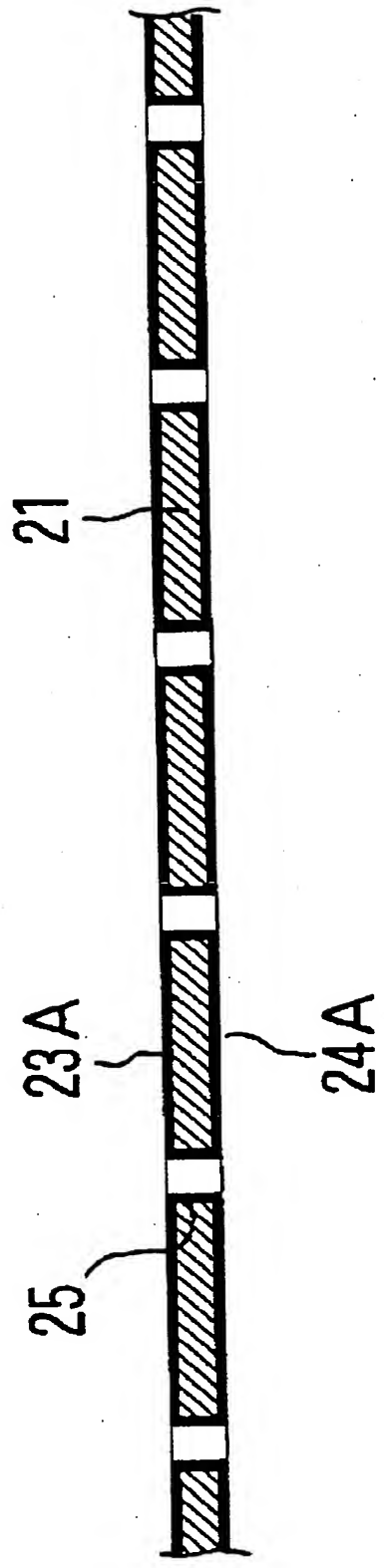


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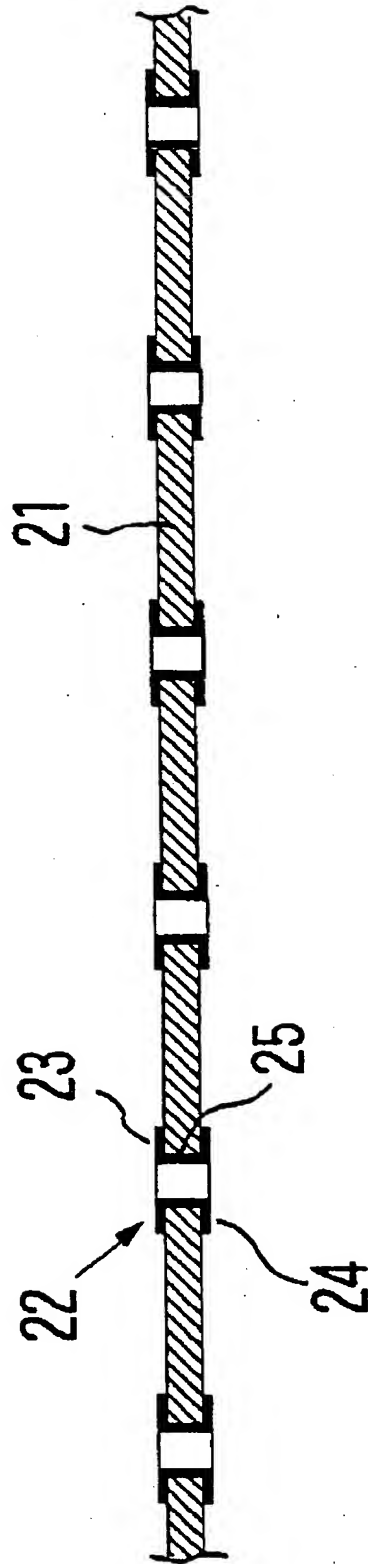


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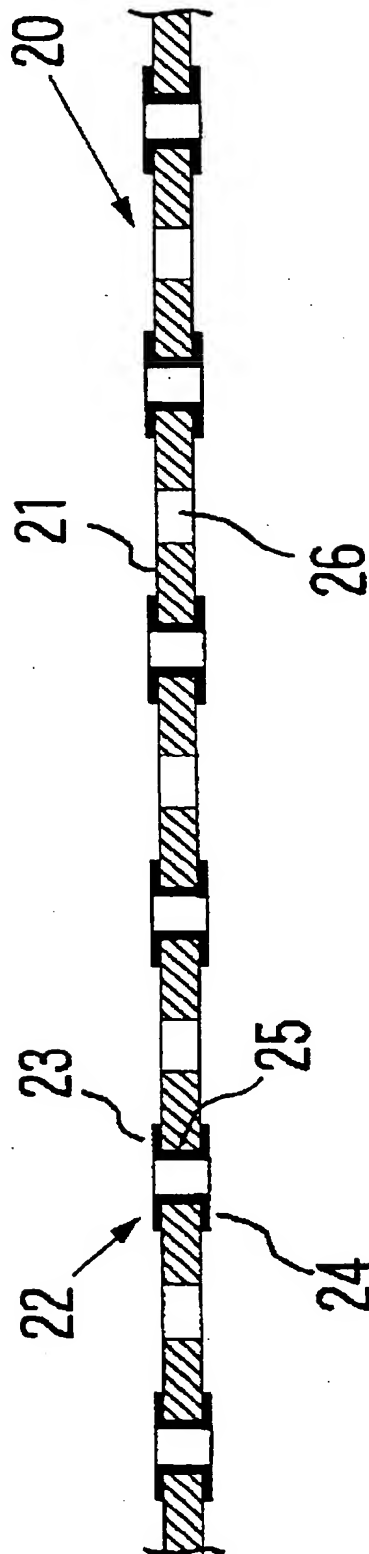


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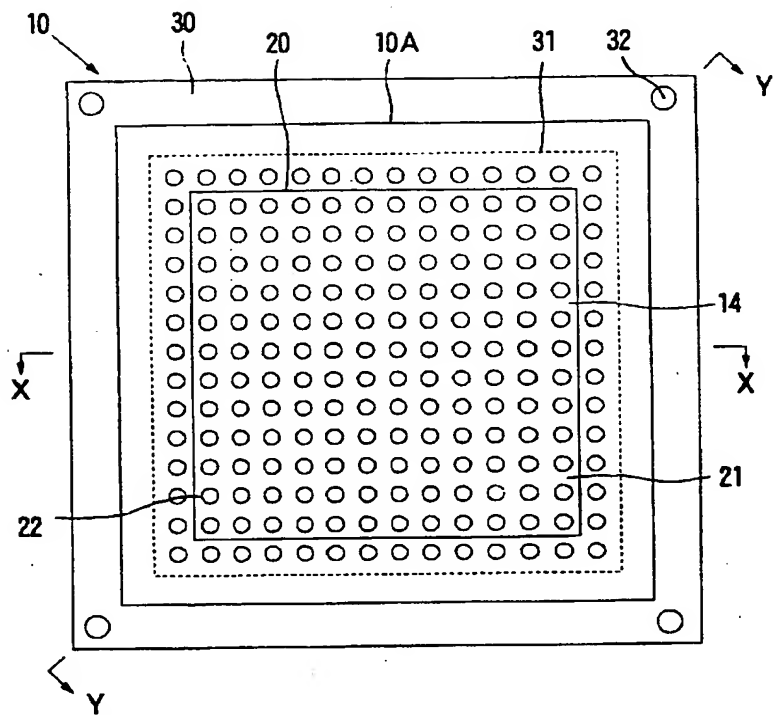
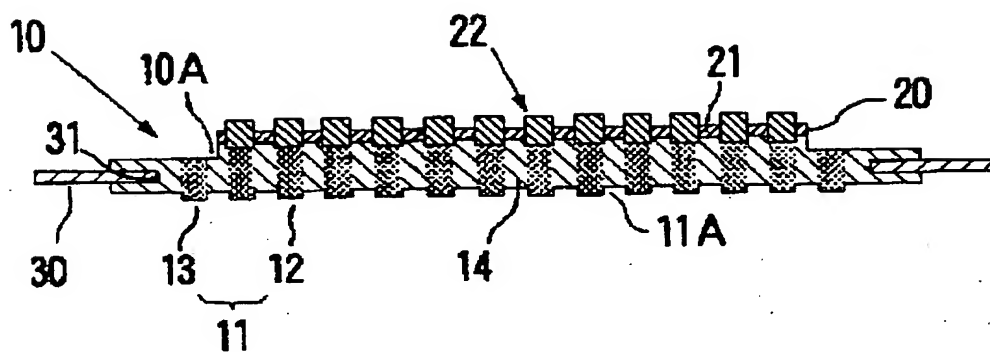


Fig. 27



A cross-sectional view of a semiconductor device. The device includes a substrate 10 with a top layer 30. A patterned layer 31 is formed on the substrate. A series of stacked layers 11, consisting of layers 12, 13, and 14, form a gate stack 20. A passivation layer 21 covers the top surface, and a contact pad 22 is provided.

Fig. 30

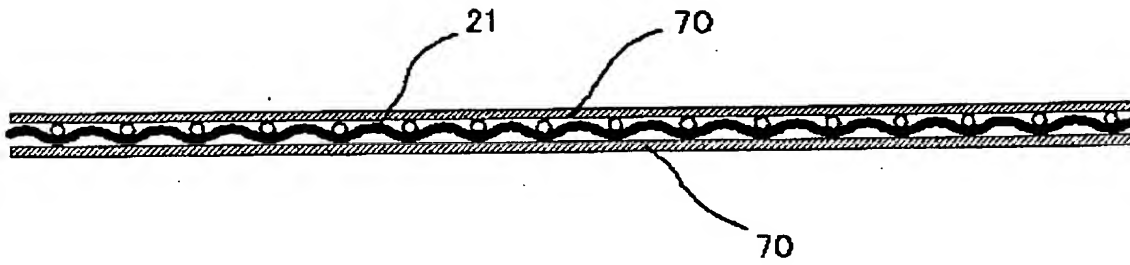


Fig. 31

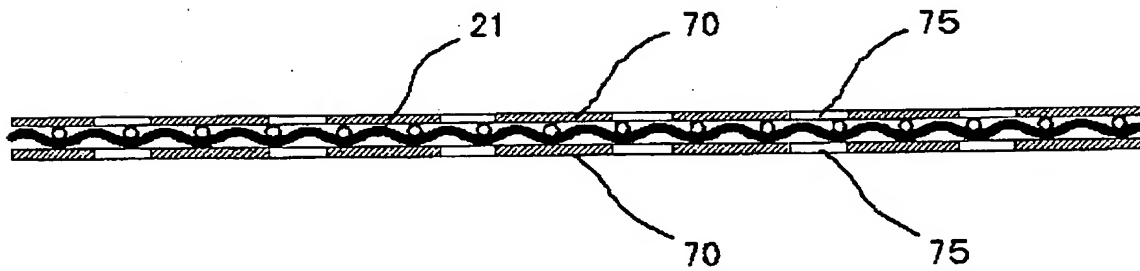


Fig. 32

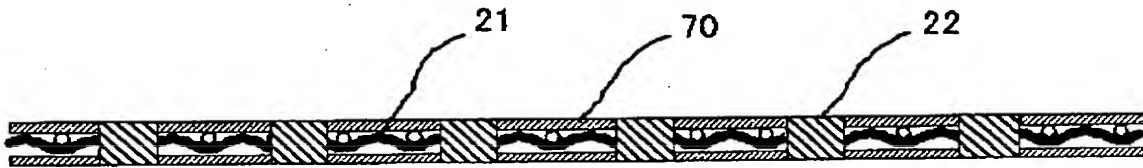


Fig. 33



Fig. 34

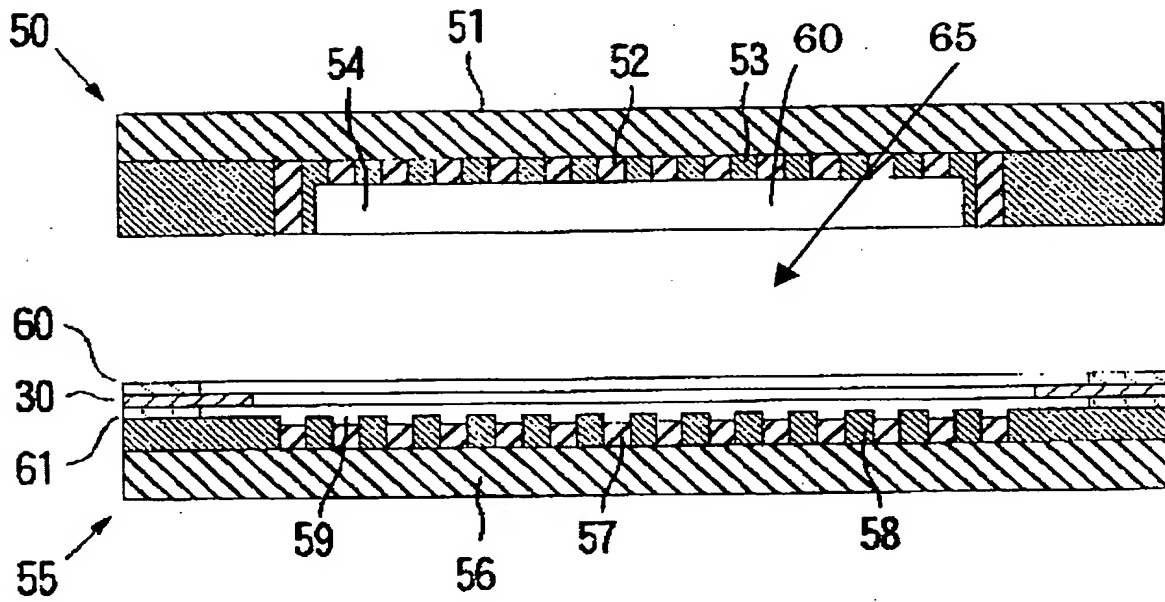


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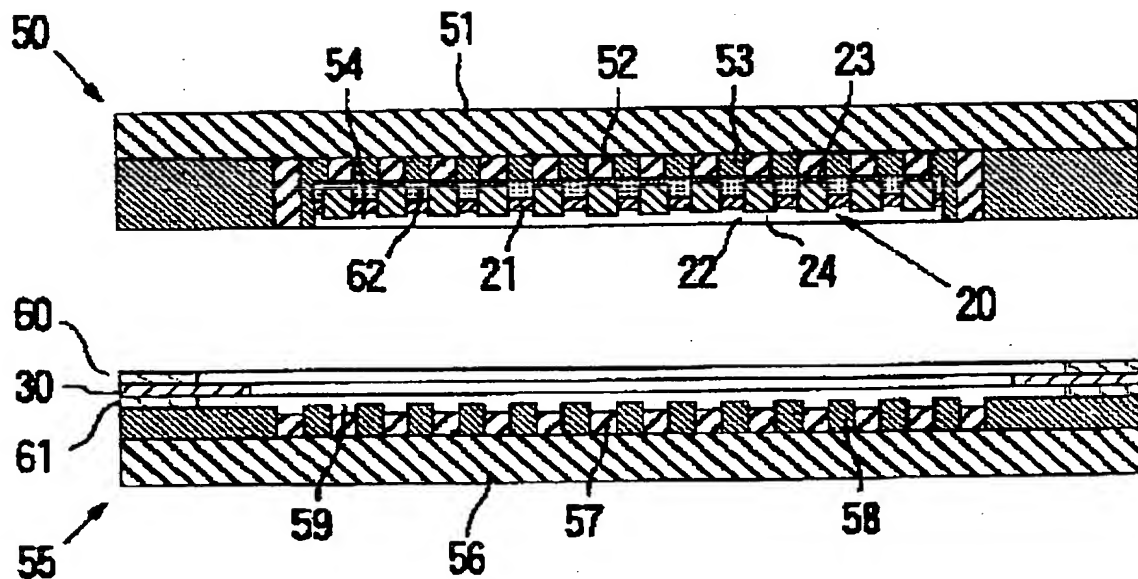


Fig. 36

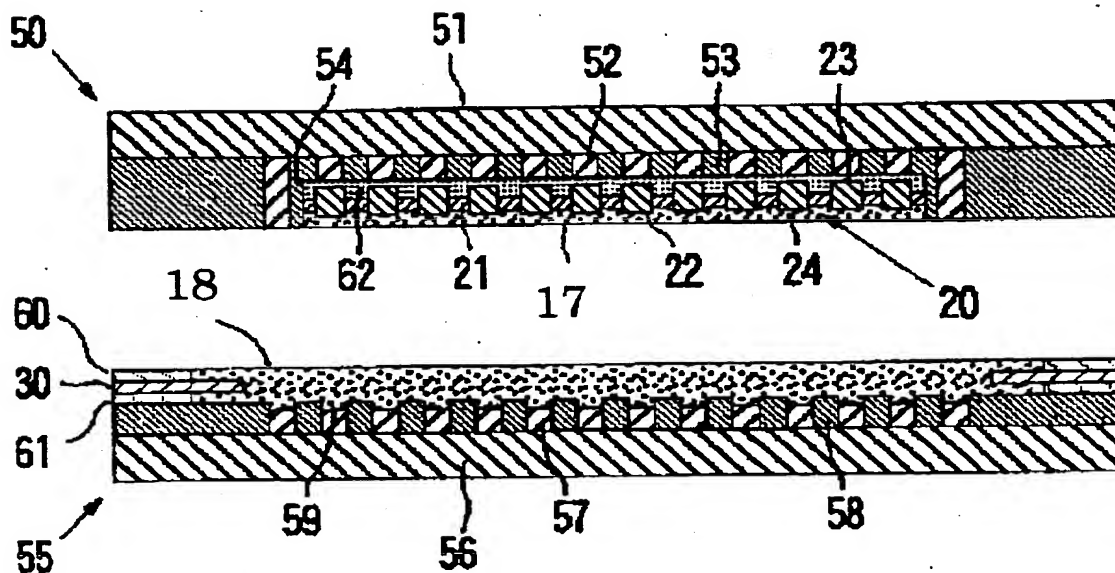


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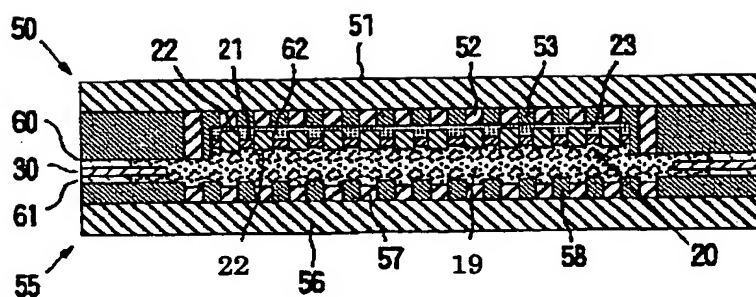


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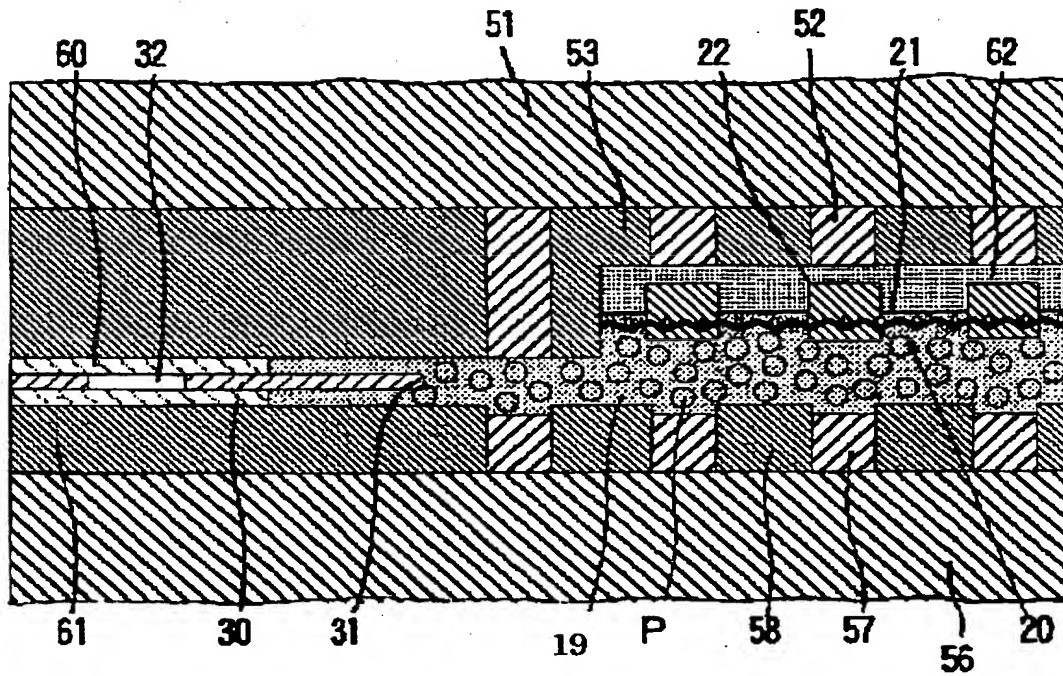


Fig. 39

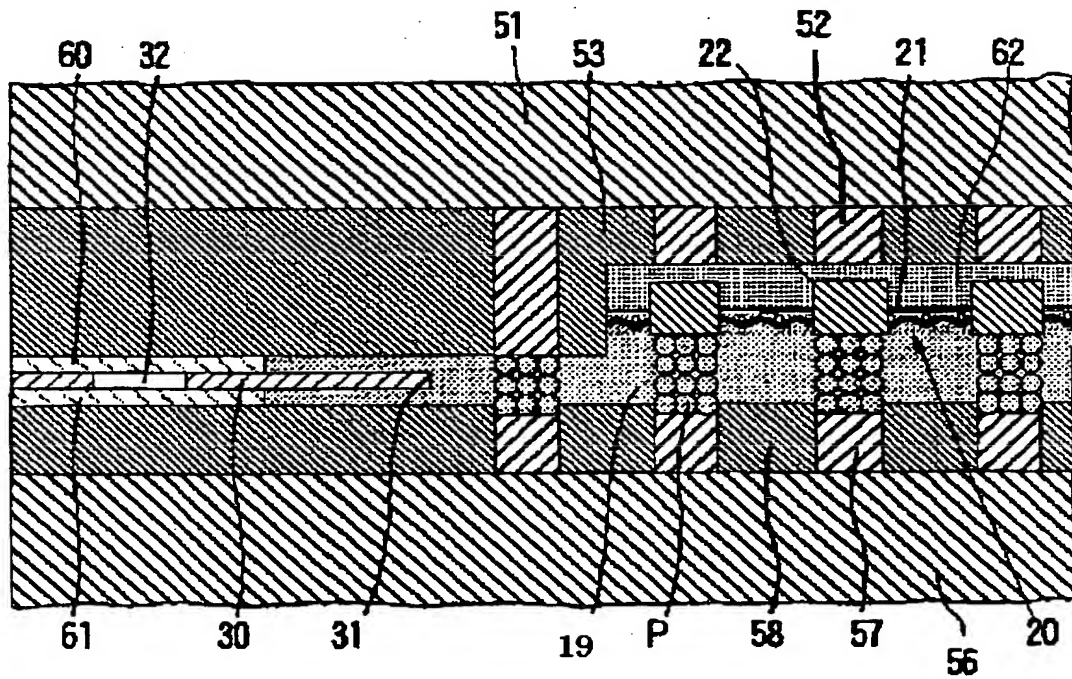


Fig. 40

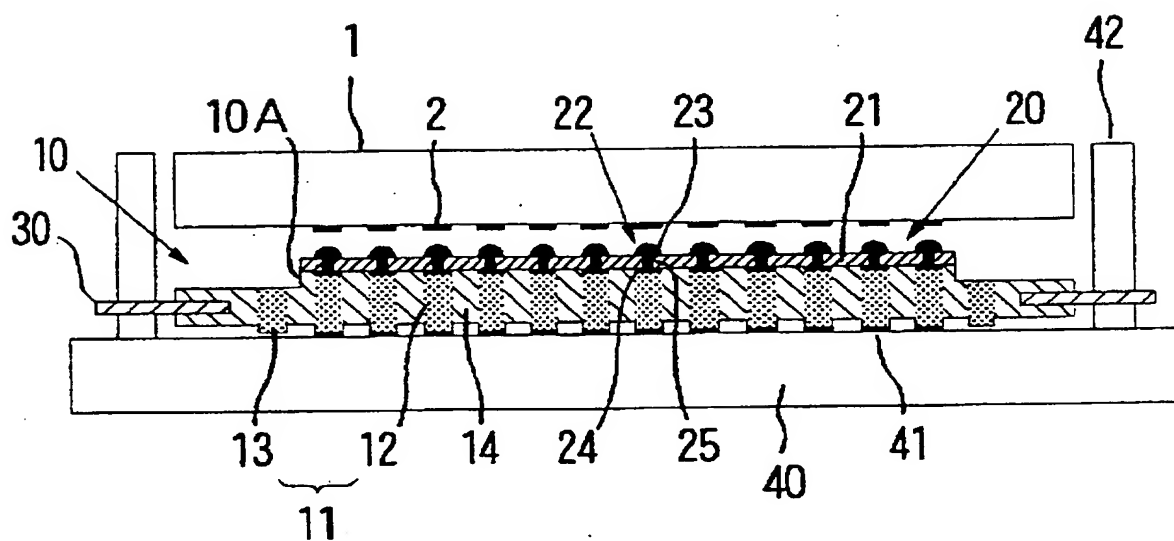


Fig. 41

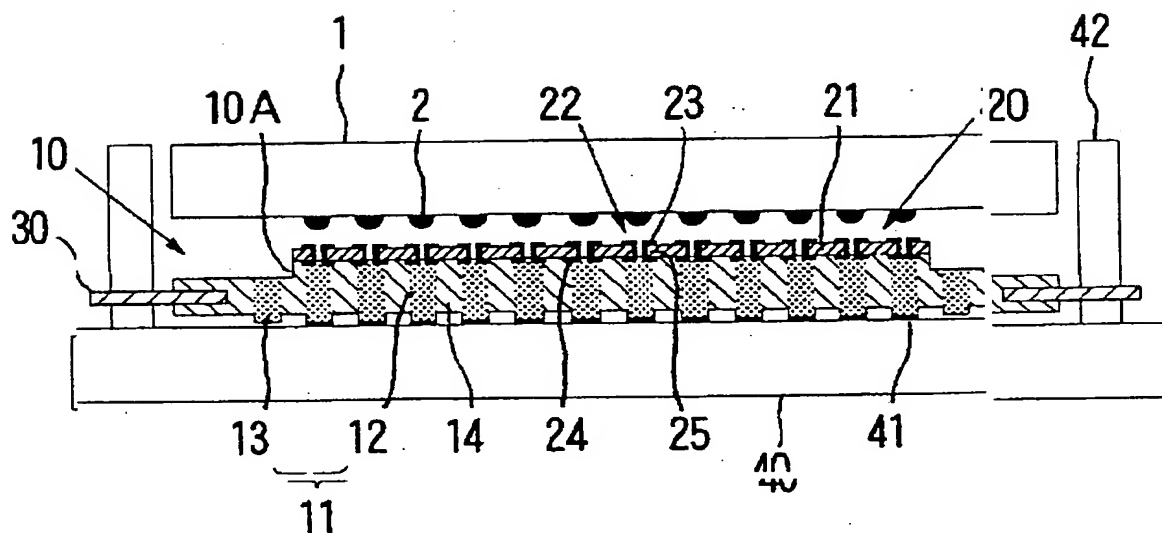


Fig. 42

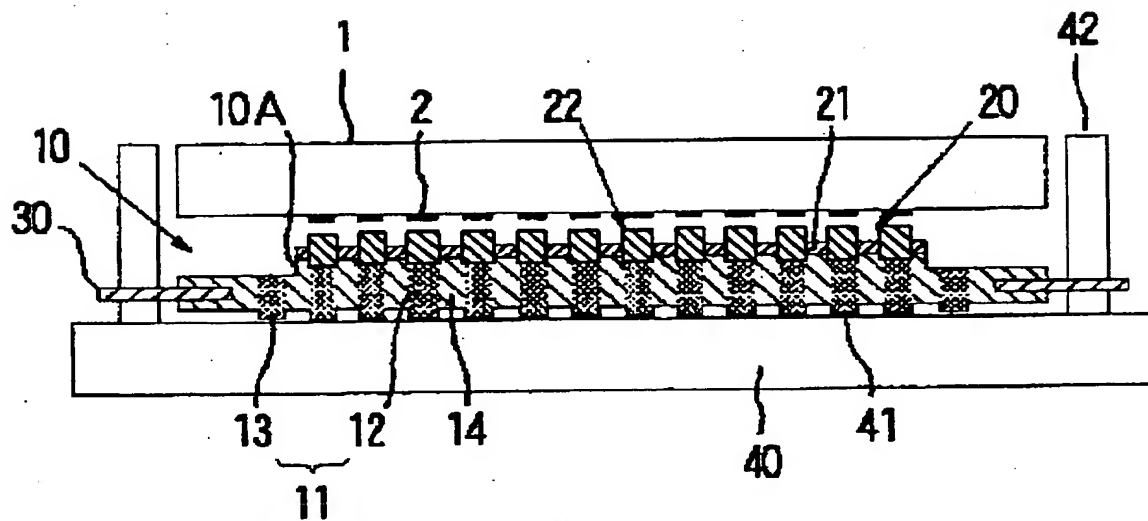


Fig. 43

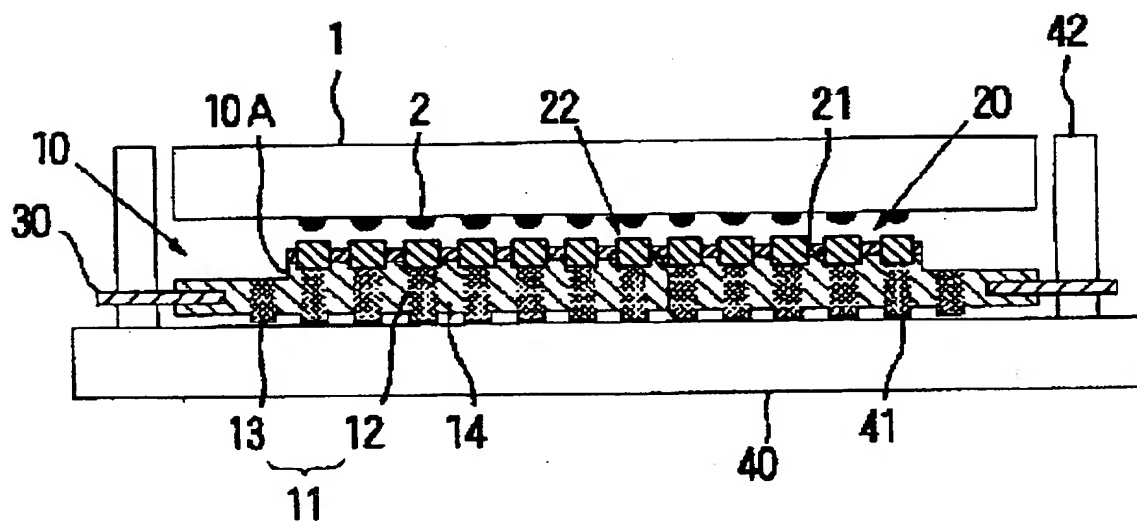


Fig. 44

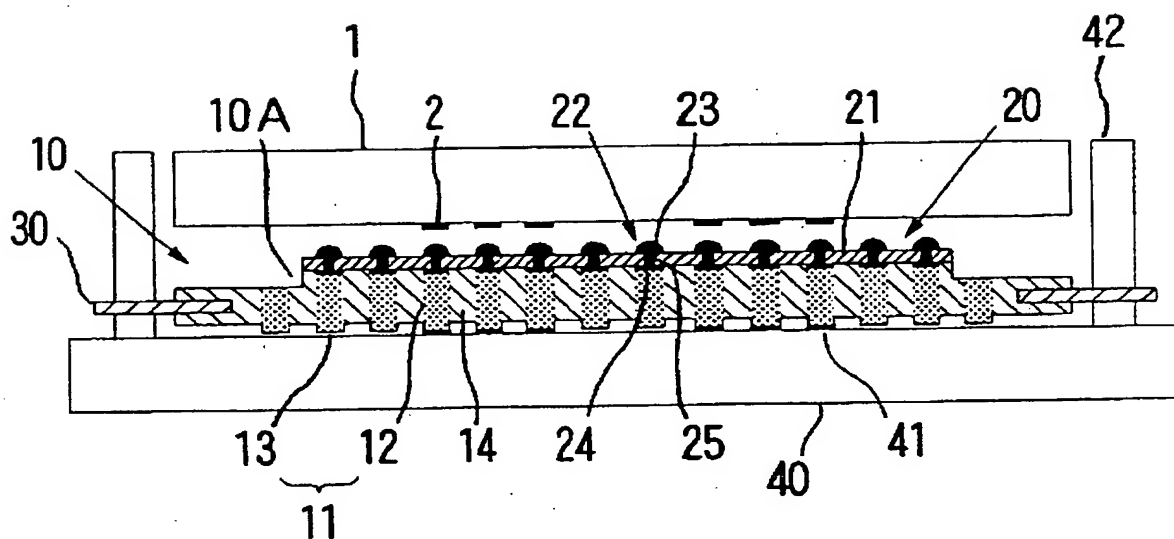


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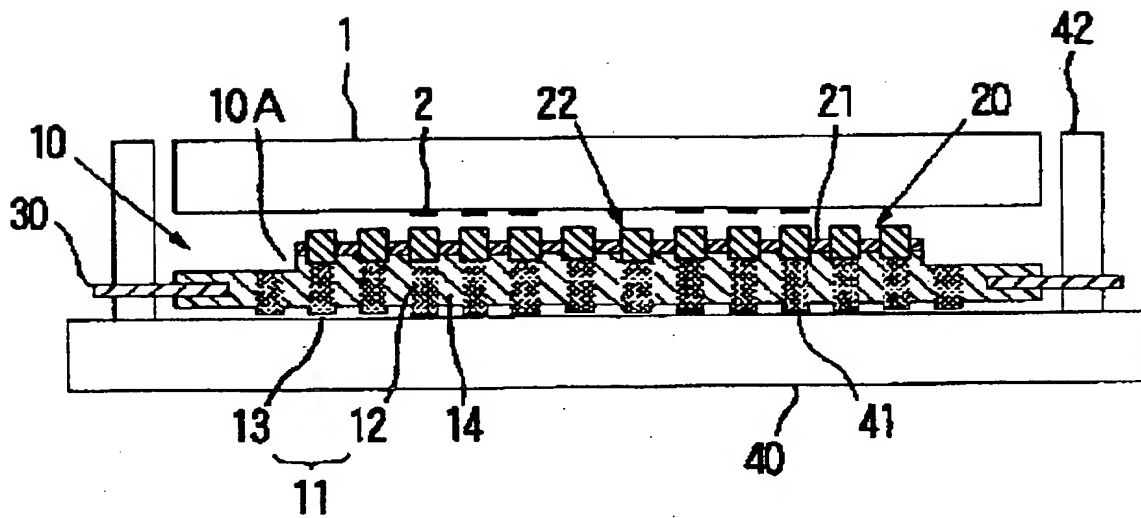


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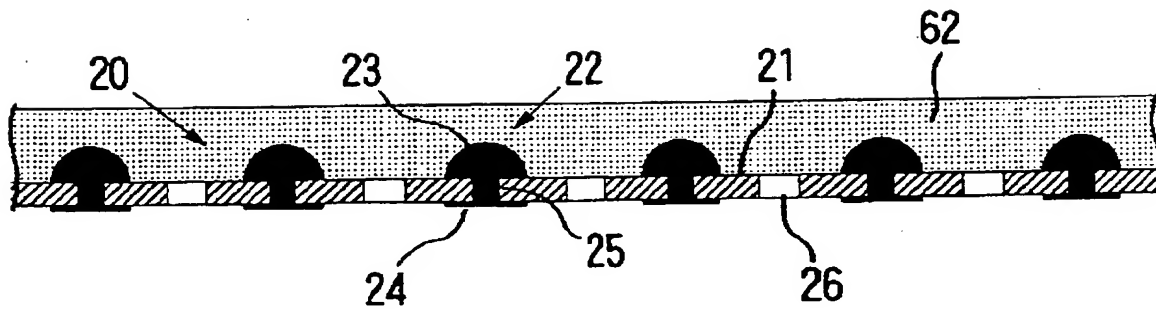


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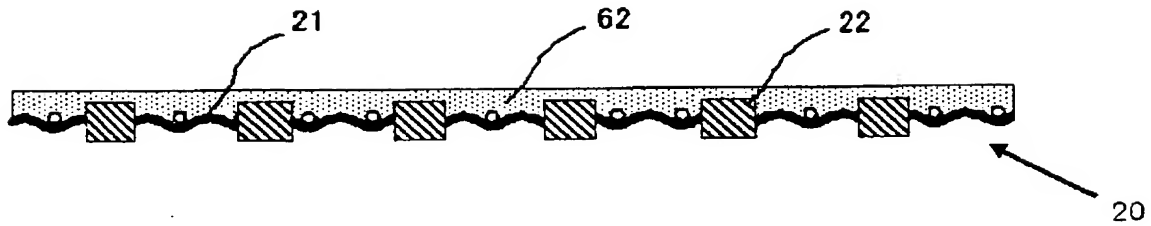


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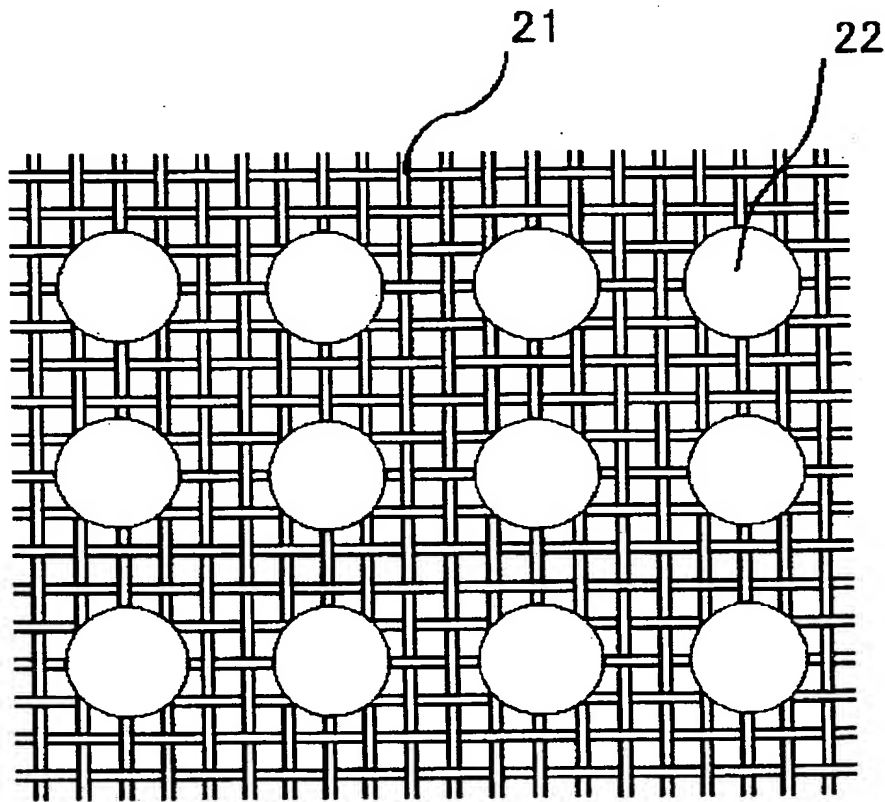


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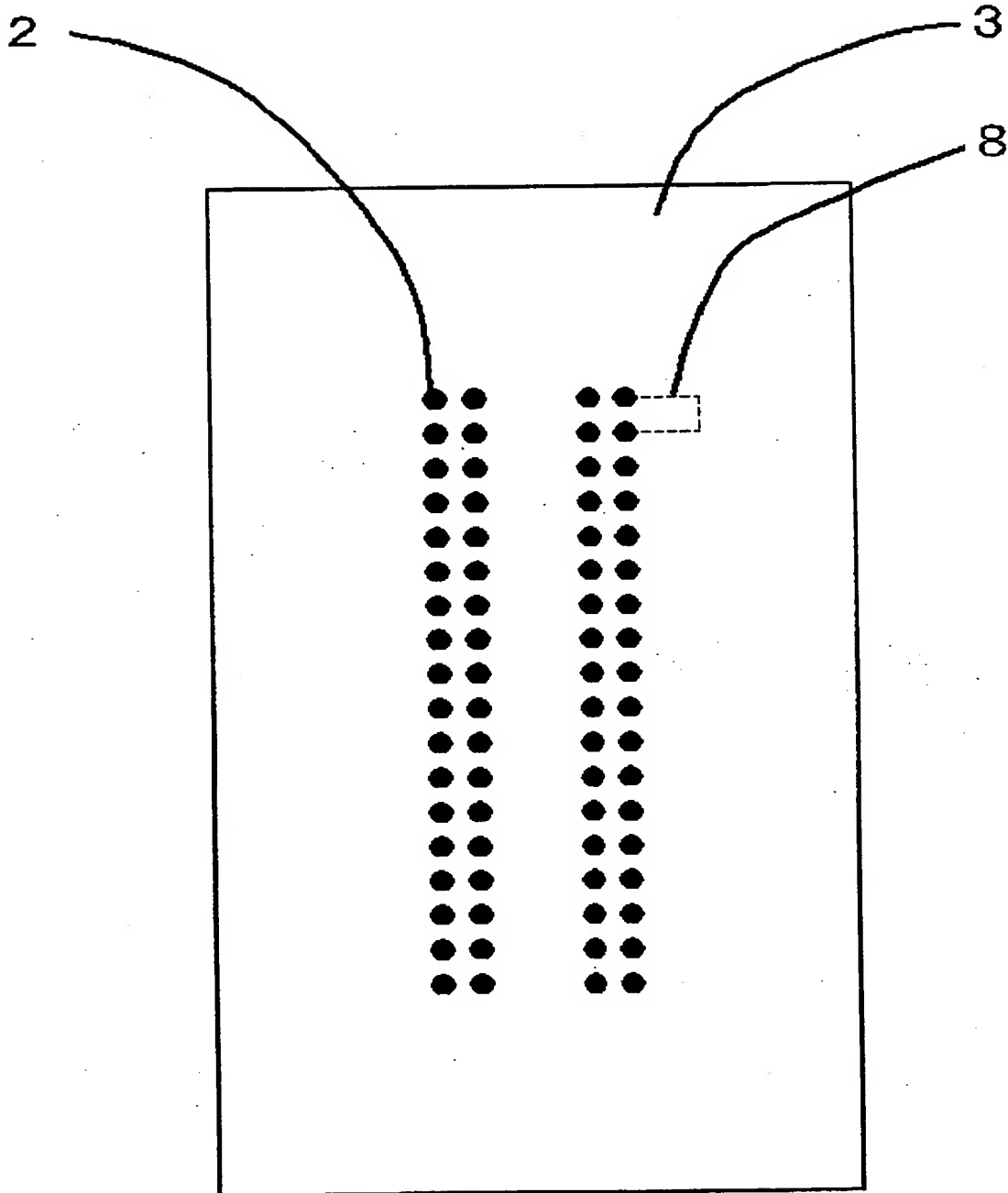


Fig. 50

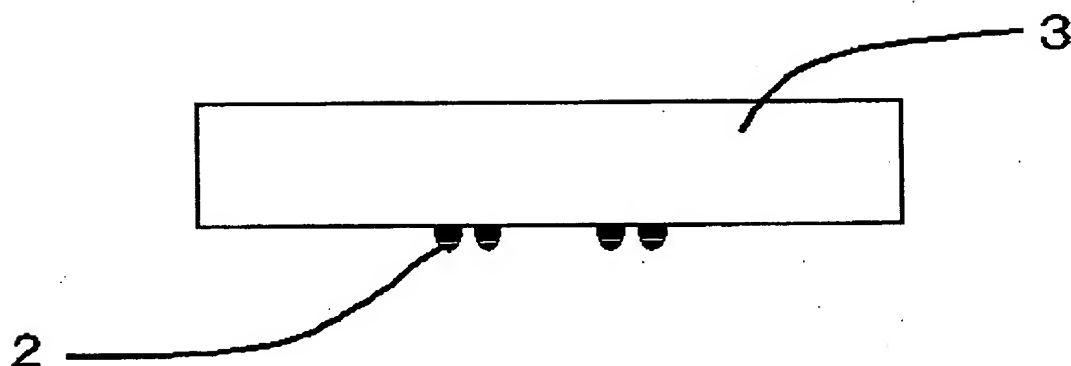
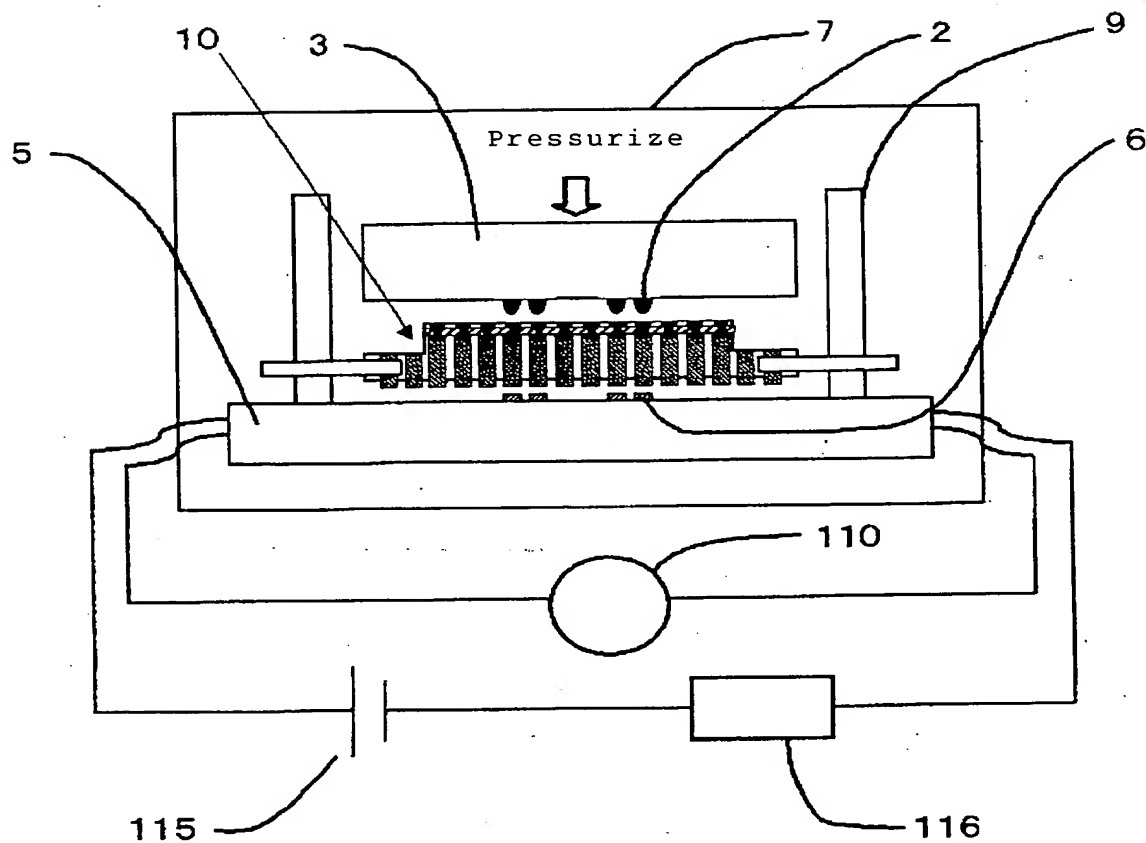


Fig. 51



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